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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/183,389	10/29/1998	VLADIMIR BEREZIN	08305/048001	3070

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EXAMINER	
WHIPKEY, JASON T	
ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/183,389	BEREZIN, VLADIMIR	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 1, 2004, has been entered.

Response to Arguments

2. Applicant's arguments filed July 1, 2004, have been fully considered but they are not persuasive.

Applicant argues that in the Merrill reference, "while a pixel may be read multiple times during an integration period, the value read from the pixel may not be used" (page 11, lines 21-22). Applicant points to column 7, lines 40-61, of Merrill, where Merrill teaches that the collected photon values are compared to a predetermined value and used only if the collected photon value is greater than or equal to the predetermined value. The examiner notes, however, that Merrill also teaches that "any value can be used as the predetermined value" (column 7, lines 41-42). Therefore, a predetermined value of zero would cause every sampled value to be stored.

Additionally, Applicant argues that the memory does not "store a sample value, but rather, it stores an accumulated sum of sampled values which exceed the predetermined threshold". This method of storing, however, is only one way disclosed by Merrill. As cited in the final rejection, Merrill teaches that, "In the preferred embodiment, unit 112 stores the first and second collected photon values of cell C1 as a total value, although the first and second collected photon values of cell C1 may alternately be stored in separate locations" (column 8, lines 51-54). In other words, Merrill teaches that sampled values may be stored individually and need not be stored as a single accumulated total.

Drawings

3. The proposed drawing correction filed July 1, 2004, is approved. In order to avoid abandonment, the drawings must now be corrected.

Specification

4. The amendment to the specification is approved and the corresponding objection withdrawn.

Claim Rejections - 35 USC § 112

5. The rejection of claims 9-17, 22, and 23 under 35 U.S.C. 112, second paragraph, has been withdrawn in response to Applicant's amendment to the specification and drawings.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9, 10, 15-22, 24, and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum (U.S. Patent No. 5,665,959) and further in view of Gray (U.S. Patent No. 5,856,829).

Regarding claims 9, 18, and 21, Merrill teaches that an active pixel cell 200 may be formed on a substrate 210, shown in Figure 7 (column 11, lines 45-46). Cell 200 is a schematic view of cell 110 shown in Figure 3 (column 11, lines 40-42). Merrill shows an imaging system 100 in Figure 2 with an array of active pixel sensor cells 110 (column 4, lines 43-53). Detection circuits DC1-DCm (an "analog to digital converter") digitize integration voltages placed on cell output lines CO1-COm by pixel cells 110 (column 7, lines 27-29). The digitized voltages are then output to memory unit 112 ("a digital memory array") (column 7, lines 27-31). The process repeats, as pixel cells 110 are read multiple times during each integration cycle (column 6, lines

53-62, and column 8, lines 23-27). Voltages may be stored in memory unit 112 as a total accumulation for each pixel cell 110 or as individual partial integration values (column 8, lines 51-54).

Merrill is silent with regard to placing the active pixel cells on the same substrate as the memory.

Fossum discloses a focal plane array 12 with CMOS pixels (column 6, lines 15-18) and a buffer memory 23, shown in Figure 7. The system shown in Figure 7 may be monolithic (column 9, lines 52-54). As stated in column 9, lines 63-65, the advantage to using a monolithic architecture is that performance is increased. For this reason, it would be obvious to have Merrill's system formed on a single substrate.

Both Merrill and Fossum are silent with regard to including a plurality of digital memory arrays.

Gray discloses a video display system with, as shown in Figure 1A, digital memory units 130 and 131 in parallel. Audiovisual data is alternately written between the two memory units (column 16, lines 40-43). As stated in column 17, lines 11-18, an advantage to using such a parallel memory structure is that multiple requests may be simultaneously made of a centralized memory. This allows for an increase in the overall processing speed of the processors dependent on the memory. For this reason, it would have been obvious at the time of invention for Merrill's and Fossum's systems to include a plurality of digital memory arrays.

Regarding claims 10 and 19, Merrill is silent with regard to using CMOS pixels.

Fossum teaches that focal plane array 12 is made up of CMOS pixels (column 6, lines 15-18). An advantage to using a CMOS image sensor is that they are easily produced using

common semiconductor fabrication techniques. For this reason, it would have been obvious at the time of invention to have Merrill's system include a CMOS image sensor.

Regarding claim 15, Merrill shows in Figure 2 that each column line CO1-COm is connected to one of the detection circuits DC1-DCm (column 4, lines 62-67).

Claim 16 may be treated like claim 9. However, Merrill is silent with regard to including a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Official Notice is taken that digital signal processing is commonly performed on pixel data before it is stored in memory. An advantage to performing DSP is that image quality may be improved. For this reason, it would have been obvious at the time of invention to have Merrill include a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Regarding claim 17, Merrill teaches that unit 112 outputs a total pixel output voltage for each cell after the entire integration period is complete (column 9, lines 29-35).

Regarding claims 20 and 24, Merrill teaches that unit 112 outputs a total pixel output voltage for each cell after the entire integration period is complete (column 9, lines 29-35).

Regarding claim 22, Gray shows in Figure 1A that his video system includes two digital memory units, 130 and 131.

Claim 26 may be treated like claim 21. However, Merrill is silent with regard to including a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Official Notice is taken that digital signal processing is commonly performed on pixel data before it is stored in memory. An advantage to performing DSP is that image quality may be improved. For this reason, it would have been obvious at the time of invention to have

Merrill include a digital signal processor between detection circuits DC1-DCm and memory unit 112.

Merrill is also silent with regard to using an analog signal processor between the image sensor and the A/D converter and placing it on the same substrate.

Fossum discloses a system comprised of CMOS pixels in focal plane array 12 (column 6, lines 15-18), digital counters 21 that perform A/D conversion (column 9, lines 26-27), and a memory 23, as shown in Figure 7. Each pixel has self-biasing circuitry to reduce reset noise ("an analog signal processor") (column 8, lines 44-47). Noise is therefore reduced after the image is sensed but before digital counters 21 digitize the signal. The advantage to reducing a signal's noise before digitizing the signal is that the digital signal produced is a more accurate representation of the intended image. For this reason, it would have been obvious to have Merrill's system implement noise reduction circuitry before digitizing the signals.

Fossum also discloses that all of the above-mentioned circuits, shown in Figure 7, may be monolithic (column 9, lines 52-54). As stated in column 9, lines 63-65, the advantage to using a monolithic architecture is that performance is increased. For this reason, it would be obvious to have Merrill's system formed on a single substrate.

8. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum and further in view of Gray and Mandl (U.S. Patent No. 5,248,971).

Claim 11 may be treated like claim 9. However, Merrill is silent with regard to detection circuits DC1-DCm being an oversampling converter.

Mandl shows in Figures 3A and 3B a video camera that uses an oversampling A/D converter (column 4, line 67 through column 5, line 3). A/D converter 144 in Figure 3B digitizes charges from array column 156 (column 5, line 67 through column 6, line 16). The charges from array column 156 are oversampled (column 6, lines 50-56).

As stated in column 10, lines 14-20, an oversampling A/D converter in an imaging system improves image quality. For this reason, it would have been obvious to have Merrill's system utilize an oversampling A/D converter.

9. Claims 12-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum and further in view of Gray and Lee (U.S. Patent No. 6,466,265).

Claim 12 may be treated like claim 9. However, Merrill is silent with regard to including an analog signal processor including analog double sampling circuitry.

Lee discloses an active pixel sensor, as shown in Figure 2e. Pixel data is sent via each column bus to a correlated double sampling circuit 91 (column 4, lines 24-27).

An advantage to performing double sampling on an image signal is that noise is reduced, resulting in an image of better quality. For this reason, it would have been obvious at the time of invention for Merrill to include double sampling circuitry in his image sensor.

Regarding claim 13, Lee teaches that the double sampling circuitry receives a reset sample ("a reference") and a signal sample from an active pixel (column 5, lines 36-43). It is inherent that correlated double sampling circuitry decreases fixed pattern noise.

Regarding claim 14, Lee shows in Figure 4 that the analog processing performed on the column pixel signals includes amplification by programmable gain amplifier 93 (column 5, lines 23-35). Programmable gain amplifier may use a variable gain element (column 5, lines 52-54). An advantage to using a variable gain amplifier is that the gain of the pixel signals may be adjusted to reach a uniform value based on lighting conditions. For this reason, it would have been obvious at the time of invention to have Merrill's image sensor include a variable gain amplifier.

10. Claims 23 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum and further in view of Gray and Berger (U.S. Patent No. 4,453,177).

Claims 23 and 25 may be treated like claims 22 and 18, respectively. However, Gray is silent with regard to placing the two memory arrays on opposite sides of the image sensor. Berger discloses a photosensitive matrix 1, as shown in Figure 2. Memories 27 and 29 are located on opposite sides of matrix 1 (column 4, lines 15-17). As stated in column 4, lines 44-47, an advantage to using such a configuration is that the luminance and chrominance components of an image signal are more easily separated. For this reason, it would have been obvious at the time of invention to have Gray's device include the two memory arrays on opposite sides of the image sensor.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW
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August 23, 2004

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PRIMARY EXAMINER